The lost silicon process

Michael Sailor, professor of chemistry at University of California, San Diego, and his team have developed a way to transfer the optical properties of silicon sensors, once thought to be the exclusive domain of "nanostructured" crystalline materials, such as porous silicon, to a variety of organic polymers.

Silicon's downside is that it is not particularily biocompatible, not flexible and it can corrode, says Sailor. "You need something that possesses all three traits if you want to use it for medical applications. You also need something that's corrosion resistant if you want to use it as an environmental sensor. This is a new way of making a nanostructured material with the unique optical properties of porous silicon, combined with the reliability and durability of plastics."

The process first starts by treating a silicon wafer with an electrochemical etch to produce a porous silicon chip containing a precise array of nanometer-sized holes. This gives the chip the optical properties of a photonic crystal-a crystal with a periodic structure that can precisely control the transmission of light, much as a semiconductor controls the transmission of electrons. The scientists then cast molten or dissolved plastic into the pores of the finished porous silicon photonic chip. The silicon chip mold is dissolved away, leaving behind a flexible, biocompatible "replica" of the porous silicon chip.

Organic chemical deposition

Nanolayers Ltd, an organic semiconductor technology company, has become the first company to receive funding approval from Israel's new 'Heznek' programmr, administered by the Office of the Chief Scientist. Millennium Materials Technology Fund, Nanolayers' lead investor, spearheaded the application. The Nanolayers technology was developed by Dr. Shlomo Yitzchaik of The Hebrew University of Jerusalem and licensed exclusively to Nanolayers by its technology transfer arm, Yissum.

The 'Heznek' programme is an innovative government programme that matches investments dollar-for-dollar, up to $1m, made by qualified Venture Capitalists. Millennium was amongst the first Funds to qualify. The government shares can subsequently be acquired by the investors, at the initial price, at any time within five years.

Nanolayers possesses a new organic chemical deposition process that has the ability to create functional electronic components one molecular layer at a time. These layers exhibit properties that compare with, and even surpass important elements of current inorganic manufacturing technology. Initial applications include flat panel displays and computer chips.

Cost-effective high-Q inductors

IMEC, Europe's microelectronics R&D center, has introduces wafer-level packaging techniques on top of back-end-of-line IC processes, to realise cost-effective high-Q inductors. The technology is of particularly interest for RF and micro wave systems.

The low quality factors (typically 5 to 10) of traditional on-chip inductors are a roadblock in the further development of silicon-based technologies at RF and microwave frequencies. IMEC has developed a new technique for the realisation of inductors on top of processed ICs: by post-processing wafer-level thin-film layers of Cu metallisation and low-k dielectrics on top of the passivation of five metal layer back-end-of-line Cu/oxide wafers where Q-factors above 30 can be obtained.

Target frequencies of the thin-film inductors cover the 1 to 20GHz frequency range. A 1nH spiral inductor with a Q factor topping 30 in a frequency range from 2.6GHz to 8.6GHz has been demonstrated with a peak Q of 38 around 4.7GHz and resonance frequency of 29GHz. The combination of post-processed passives with patterned ground shields underneath spiral inductors, further increases the Q factor and significantly extends the performance of the spiral inductors towards higher frequencies.

The post-processing is compatible with both Al and Cu back-end with no performance shift in the underlying interconnect layers and devices. Thin-film wafer-level packaging means the solution is cost effective and consumes no additional silicon real estate. Models for the inductors are available enabling co-design of post-processed inductors and the RF circuit.

Using this technique, IMEC has created opportunities for cost-effective highly-integrated high-performance RF and microwave ICs. These can be mounted and interconnected using IMEC's multi-layer TFT to produce high-performance miniature system-in-a-package solutions for wireless telecoms applications.

Seiko and SOI

Japanese Seika is exclusive distributor in China for products based on Soitec's Smart Cut technology. Seika will staff its Shanghai office with a sales-force dedicated to Soitec's offerings. The new agreement builds on a ten-year distribution partnership between the two companies. Soitec believes that it is the first SOI company to establish a sales and customer support base in China.

Andre Auberton-Herve, Soitec president and CEO, says the deal "will help us reach new customers and markets - not only with our Unibond wafers, but also with future products, currently in development, based on advanced new substrates."

SiGen SOI for opto

Silicon-on-insulator (SOI) wafer supplier Silicon Genesis Corporation has secured a blanket order to provide substrates for integrating single chip optoelectronics into standard silicon chip processing. The product has been qualified. SiGen believes the collaboration has the potential to lead to large wafer volumes from the technology for optically enabled VLSI products.

Silicon on Insulator Tecnologies (Soitec) however has been awarded $3m in its US patent suit against Silicon Genesis when a jury in the District Court of Massachusetts awarded the damages after concluding that SiGen had infringed a key claim in a patent covering technology in Soitec's "Smart Cut" technology for silicon-on-insulator wafers.